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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Won Sun Shin et al.  
Assignee: Amkor Technology, Inc.  
Title: SEMICONDUCTOR PACKAGE AND METHOD FOR FABRICATING THE SAME  
Serial No.: 10/825,670 Filing Date: April 14, 2004  
Patent No.: RE40,112 Issued: February 26, 2008  
Examiner: Chuong A. Luu Group Art Unit: 2818  
Docket No.: GK0012RI

Monterey, CA  
October 9, 2008

ATTENTION: CERTIFICATE OF CORRECTIONS BRANCH  
COMMISSIONER FOR PATENTS  
P.O. BOX 1450  
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**Certificate**  
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of Correction

REQUEST FOR ENTRY OF  
CERTIFICATE OF CORRECTION

Sir:

Please enter the enclosed Certificate of Correction (PTO Form 1050) in the above patent.

The errors sought to be corrected were made by

- ☒ The Patent and Trademark Office as explained below. Thus, no fee is required for the Certificate of Correction pursuant to 37 CFR §1.322.
- ☐ Applicant(s) (at least in part). See next section for explanation. This appropriate fee under 37 CFR §1.323 has been authorized below.

Attached as Exhibit A (3 pages) is a copy of the relevant pages of the Claims as filed with the original application on May 19, 2000, which supports the requested correction to Claims 3, 19 and 26 and shows that the errors were made by the U.S. Patent and Trademark Office.

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As shown in Exhibit A, Line 14 of Claim 3 reads "...ones of the first ball lands". The same line in the patent at Column 13, Line 49 reads "...ones of the ball lands". Specifically, the word "first" was incorrectly omitted from the Claim.

As also shown in Exhibit A, Line 3 of Claim 19 reads "...all of the unit circuit boards...". The same line in the patent at Column 15, Line 3 reads "...all of the unit circuit board...". Specifically, the word "board" should be replaced with the word --boards--.

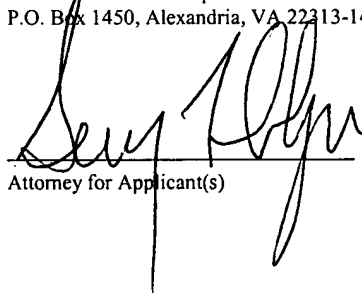
As further shown in Exhibit A, Line 4 of Claim 26 reads "...one of which has cavities and gates...". The same line in the patent at Column 16, Line 10 reads "...one or which has cavities and gates...". Specifically, the word "or" should be replaced with the word --of--.

The Commissioner is hereby authorized to charge any fees required for consideration and entry of the enclosed documents, and to credit any overpayment of fees to Deposit Account No. 50-0553.

Please direct all inquiries concerning this request to the undersigned attorney.

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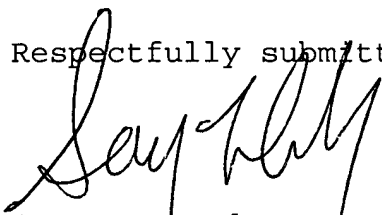
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 9, 2008.



Attorney for Applicant(s)

October 9, 2008  
Date of Signature

Respectfully submitted,



Serge J. Hodgson  
Attorney for Applicant(s)  
Reg. No. 40,017  
(831) 655-0880

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1 3. The method of claim 1, wherein the circuit board  
2 strip comprises:

3 a resin substrate having a substantially rectangular  
4 strip shape provided with a first major surface and a second  
5 major surface;

6 a plurality of slots extending to a desired length and  
7 serving to divide each of the resin substrate into a  
8 plurality of substrate portions arranged in a matrix array,  
9 each of the substrate portions corresponding to one of the  
10 unit circuit boards having one of the through holes;

11 a plurality of first circuit patterns each formed on  
12 the first major surface of the resin substrate for an  
13 associated one of the strip portions and provided with  
14 associated ones of the first ball lands;

15 a plurality of second circuit patterns each formed on  
16 the second major surface of the resin substrate for an  
17 associated one of the strip portions and provided with  
18 associated ones of the bond fingers; and

19 cover coats respectively coated over the first and  
20 second major surfaces of the resin substrate while allowing  
21 the bond fingers and the ball lands to be exposed  
22 therethrough.

1 4. The method of claim 1, further comprising attaching  
2 one or more closure members to the first surface of the  
3 substrate strip so that each through hole is covered thereby  
4 prior to receiving the semiconductor chip in the respective  
5 through hole.

1 18. The method according to claim 5, wherein a unitary  
2 body of encapsulant material covers the second major surface  
3 of all of the unit circuit boards of the circuit board  
4 strip.

1 19. The method according to claim 6, wherein a unitary  
2 body of encapsulant material covers the second major surface  
3 all of the unit circuit boards of the circuit board strip.

1 20. The method according to claim 17, wherein  
2 singulating the circuit board strip is carried out in such a  
3 fashion that the encapsulant material and the circuit board  
4 strip are simultaneously split.

1 21. The method according to claim 18, wherein  
2 singulating the circuit board strip is carried out in such a  
3 fashion that the encapsulant material and the circuit board  
4 strip are simultaneously split.

1 22. The method according to claim 19, wherein  
2 singulating the circuit board strip is carried out in such a  
3 fashion that the encapsulant material and the circuit board  
4 strip are simultaneously split.

1 23. The method of claim 1, wherein encapsulating the  
2 circuit board strip comprises:

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7 into the cavity; and  
8 injecting the encapsulating material into each of the  
9 cavities through the associated gate in such a fashion that  
10 it flows outwardly from a central portion of the second  
11 major surface of the associated semiconductor chip along the  
12 second major surface, fills the through hole, and contacts  
13 the closure member.

1 26. The method of claim 9, wherein the encapsulating  
2 the circuit board strip comprises:

3 interposing the circuit board strip between a pair of  
4 mold dies, one of which has cavities and gates, in such a  
5 fashion that the second major surface of each of the  
6 semiconductor chips faces an associated cavity and a gate  
7 into the cavity; and

8 injecting the encapsulating material into each of the  
9 cavities through the associated gate in such a fashion that  
10 it flows outwardly from a central portion of the second  
11 major surface of the associated semiconductor chip along the  
12 second major surface, fills the through hole, and contacts  
13 the closure member.

1 27. The method of claim 1, wherein each unit circuit  
2 board of the circuit board strip is further provided with a  
3 plurality of second ball lands at the second major surface  
4 thereof.

1 28. The method of claim 2, wherein each unit circuit  
2 board of the circuit board strip is further provided with a

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## UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO : RE40,112

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APPLICATION NO. : 10/825,670

ISSUE DATE : February 26, 2008

INVENTOR(S) : Won Sun Shin, Do Sung Chun, Sang Ho Lee, Seon Goo Lee and Vincent Dicaprio

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 13, Line 49, Claim 3, replace "ones of the ball lands" with --ones of the first ball lands--;

In Column 15, Line 3, Claim 19, replace "the unit circuit board" with --the unit circuit boards--;

In Column 16, Line 10, Claim 26, replace "one or which" with --one of which--.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

GUNNISON, McKAY & HODGSON, L.L.P.  
1900 Garden Road, Suite 220  
Monterey, CA 93940

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary, depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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